REMARKS

Applicants thank the Patent Office for acknowledging Applicant's claim to foreign priority, and for indicating that the certified copy of the priority document, Italian Patent Application No. TO2000A 000 760 dated July 31, 2000, has been made of record in the file.

Claims 1-11 have been examined on their merits.

Applicants herein editorially amend claims 2-10 to remove awkward language and to conform the claims to U.S. practice. The amendments to claims 2-10 were made merely to more accurately claim the present invention, and were not made for reasons of patentability.

Claims 1-11 are all the claims presently pending in the application.

1. Claims 1-9 and 11 stand rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Field *et al.* (U.S. Patent No. 6,778,529). Applicants traverse the § 102(e) rejection of claims 1-9 and 11 for at least the reasons discussed below.

Field *et al.* disclose, *inter alia*, a separate asynchronous transfer mode (ATM) and time division multiplex (TDM) switch hardware at the switch core to receive and process the ATM and TDM traffic, respectively. The separate data paths and switching hardware for ATM and TDM traffic are expensive and may be cost prohibitive for some lower rate applications. Field *et al.* attempt to solve this problem by providing a synchronous switch, which uses a common data path and memory to switch both ATM and TDM traffic.

As shown in Figure 1 of Field *et al.*, integrated access devices (IADs) 14 connect customer premise equipment (CPE) 12 to a network 16. The integrated access devices 14 are

source/termination nodes and the backbone routers 18 are intermediate nodes for a connection 22 spanning across a telecommunications system 10.

As shown in Figure 2 of Field *et al.*, the integrated access device 14 comprises line cards 40, a switch core 44 and a rate adjustable backplane 46. Each line card 40 comprises one or more external ports 48, one or more internal interfaces 50 and a traffic processor 52. The ports 48 receive ingress traffic from an external line and/or transmit egress traffic received by the internal interfaces 50 from the switch core 44. The internal interfaces 50 transmit ingress traffic received by the ports 48 from the external links and received egress traffic from the switch core 44. The switch core 44 performs synchronous based switching such as TDM switching and cell based switching based on a synchronized frame pulse.

The Patent Office argues that the connection 22 in Field *et al.* teaches the data stream sent in a co-directional way. However, with respect to the present invention recited in claim 1, the second information streams are exchanged between a first circuit means and a second circuit means, and the first circuit means and the second circuit means are parts of a node. In contrast, Field *et al.* disclose that the connection 22 is between two nodes, *i.e.*, the source/termination node 14 and the intermediate node 18, instead of a data stream between parts of the same node.

The Patent Office also argues that (a) the network line card 42b of Field *et al.* discloses the second circuit means; (b) the customer line card 42a of Field *et al.* discloses the first circuit means; and (c) the internal interface 50 of Field *et al.* discloses the transport interface. However, Field *et al.* disclose that the network line card 42b is used to communicate the traffic between the network 16 and the integrated access device 14. Field *et al.* lack any teaching or suggestion that

the network line card 42b (cited by the Patent Office as disclosing the second circuit means) can return to the customer line card 42a (cited by the Patent Office as disclosing the first circuit means) data originated from the network line card 42b in response to a request from the customer line card 42a.

Based on the foregoing reasons, Applicants submit that independent claim 1 is allowable over Field *et al.*, and further submit that claims 2-9 are allowable as well, at least by virtue of their dependency from claim 1. Applicants respectfully request that the Patent Office reconsider and withdraw the § 102(e) rejection of claims 1-9.

With respect to independent claim 11, Applicants submit that independent claim 11 is allowable for at least reasons analogous to claim 1. Applicants respectfully request that the Patent Office reconsider and withdraw the § 102(e) rejection of claim 11.

In addition, with respect to claim 4, the Patent Office argues that the source/termination node 14 of Field *et al.* teaches the transmitter of claim 4. However, the transmitter of claim 4 is in the transport interface between the first circuit means and the second circuit means of a node for intra-equipment communications. In Field *et al.*, however, the node 14 is for communications between CPE 12 and the intermediate node 18. Accordingly, Field *et al.* fail to teach or suggest the transmitter, and claim 4 is allowable for this additional reason as well.

With respect to claim 5, the Patent Office argues that the intermediate node 18 of Field *et al.* teaches the receiver of claim 5. However, the receiver of claim 4 is in the transport interface between the first circuit means and the second circuit means of a node for intra-equipment communications. In Field *et al.*, however, the node 18 is for communications between the

integrated access device 14 and another intermediate node 18. Accordingly, Field *et al.* fail to teach or suggest the receiver, and claim 5 is allowable for this additional reason as well.

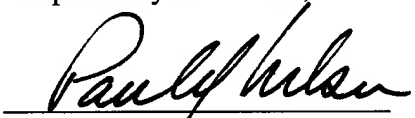
2. Claim 10 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Field *et al.* in view of Kulkarni *et al.* (U.S. Patent No. 6,414,966). Applicants respectfully traverse the § 103(a) rejection of claim 10 for at least the reasons discussed below.

Kulkarni *et al.* disclose, *inter alia*, a device that maps/demaps Ethernet traffic directly onto and from a Synchronous Optical Network (SONET). Given the different goals of Field *et al.* and Kulkarni *et al.*, there is no motivation or suggestion for a skilled artisan to combine Field *et al.* and Kulkarni *et al.* Moreover, Kulkarni *et al.* disclose a device that can be implemented on a field programmable gate array (FPGA) or an application specific integrated circuit (ASIC) to map/demap Ethernet packets to SONET data and SONET data to Ethernet packets. Thus, in Kulkarni *et al.*, FPGA and ASIC are used as two alternatives for the maping/demapping, instead of two circuit means of a node communicating with each other over a transport interface. Accordingly, Applicants respectfully submit that claim 10 is allowable over the combination of Field *et al.* and Kulkarni *et al.*, and respectfully request that the Patent Office reconsider and withdraw the § 103(a) rejection of claim 10.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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